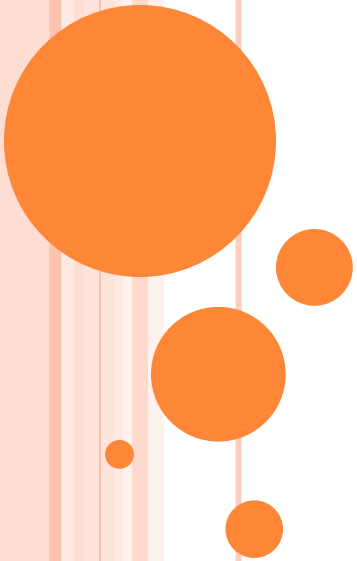


Multi-Processor Embedded Systems

Ann Melnichuk

Long Talk

Reference

Multi-Core Embedded Systems
Edited by Georgios Kornaros
CRC Press 2010Pages 1–29
Print ISBN: 978-1-4398-1161-0
eBook ISBN: 978-1-4398-1162-7
DOI: 10.1201/9781439811627-c1
http://www.crcnetbase.com/doi/book/10.1201/9781439811627

Definitions

System-on-Chip (SoC)

multiple processors
local DRAM
flash memory
hardware accelerators
RF components

Network-on-Chip (NoC)

communication subsystem between IP cores in a System-on-a-Chip (SoC)

OVERVIEW OF THE BOOK

Chapter 1

Multi-Core Architecture for Embedded Systems

- Overview of the various multi-core architectures
- Discussion about the challenges
- Will be the focus of this presentation

Chapter 2

Application-Specific Customizable Embedded Systems

- discussion about customizable processors in the context of MPSoC
- For a given embedded application:
  - special instructions
  - special functional units
  - custom data widths
  - custom register file structure

Chapter 3

Power Optimizations in MCSoC

- Power analysis tools
- Low power design
  - Dynamic power management (DPM)
  - Dynamic voltage scaling (DVS)

Power Management Methods	Pros	Cons
Clock Gating	Simple additional gating logic	Leakage power dissipation Medium power/ ground noise
Power Gating	No leakage	Complex additional p/g switching logic High power/ground noise
DVFS	Good controllability between power and performance Low p/g noise	Complex additional on-chip p/g voltage regulators required
Smart Caching	Software controlled Some level of optimization possible between power and performance	Cache logic increases Verification of coherence protocols difficult
Scheduling	Global power optimization possibly unlike all other methods Good control over p/g noise	Kernel or user code has to be changed

Chapter 4

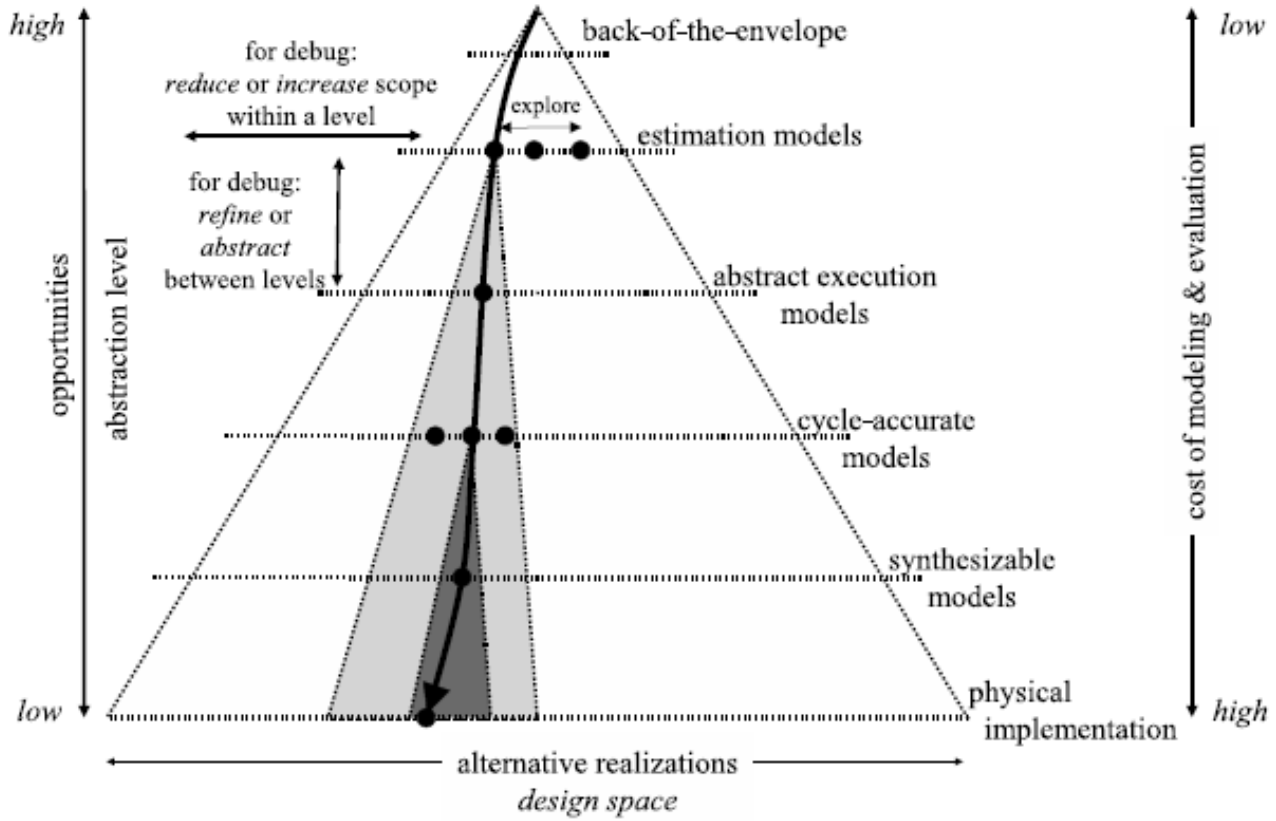
Routing Algorithms for Irregular Mesh-Based NoC

- 2D mesh NoC built with different types of cores → thus irregular
- Various routing models
- Presentation and explanation of several algorithms

Chapter 5

Debugging Multi-Core Systems-on-Chip

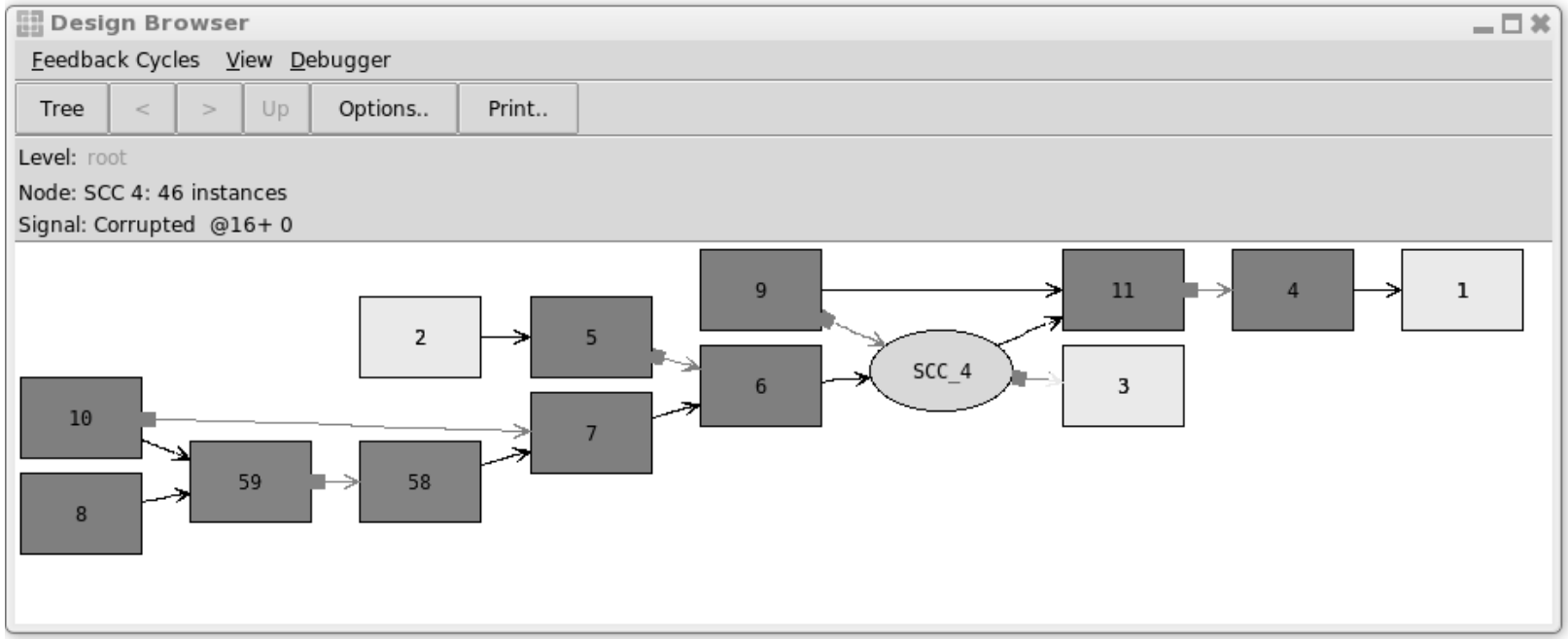
- Higher level of abstraction



Chapter 5

Debugging Multi-Core Systems-on-Chip

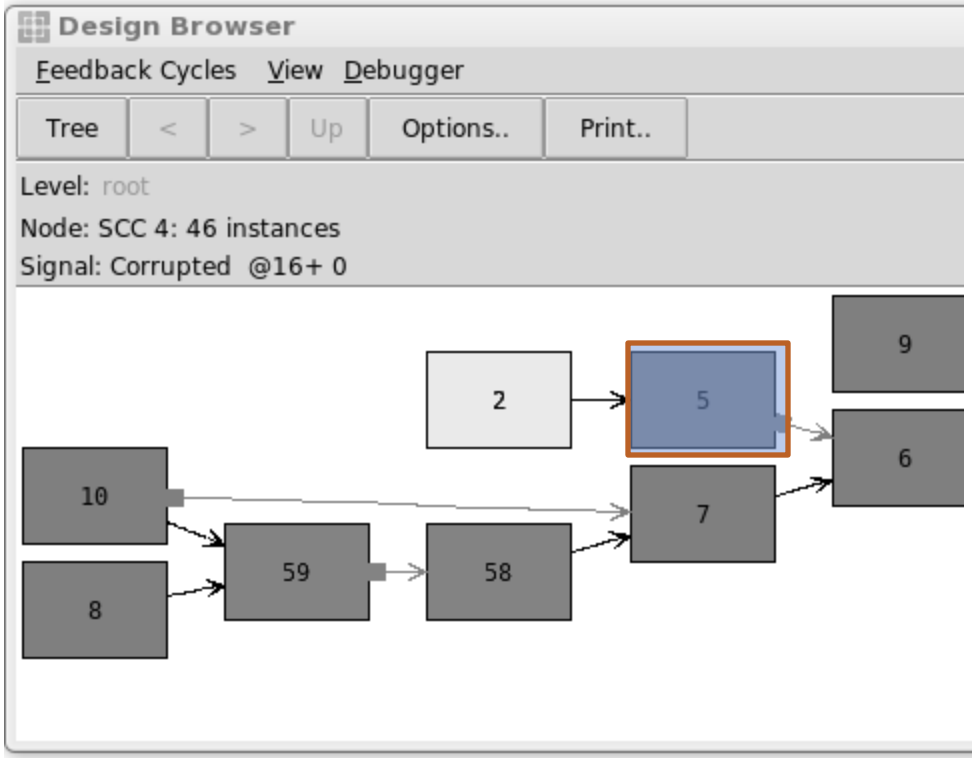
- Debugging tool which allows one to "zoom in" on the error

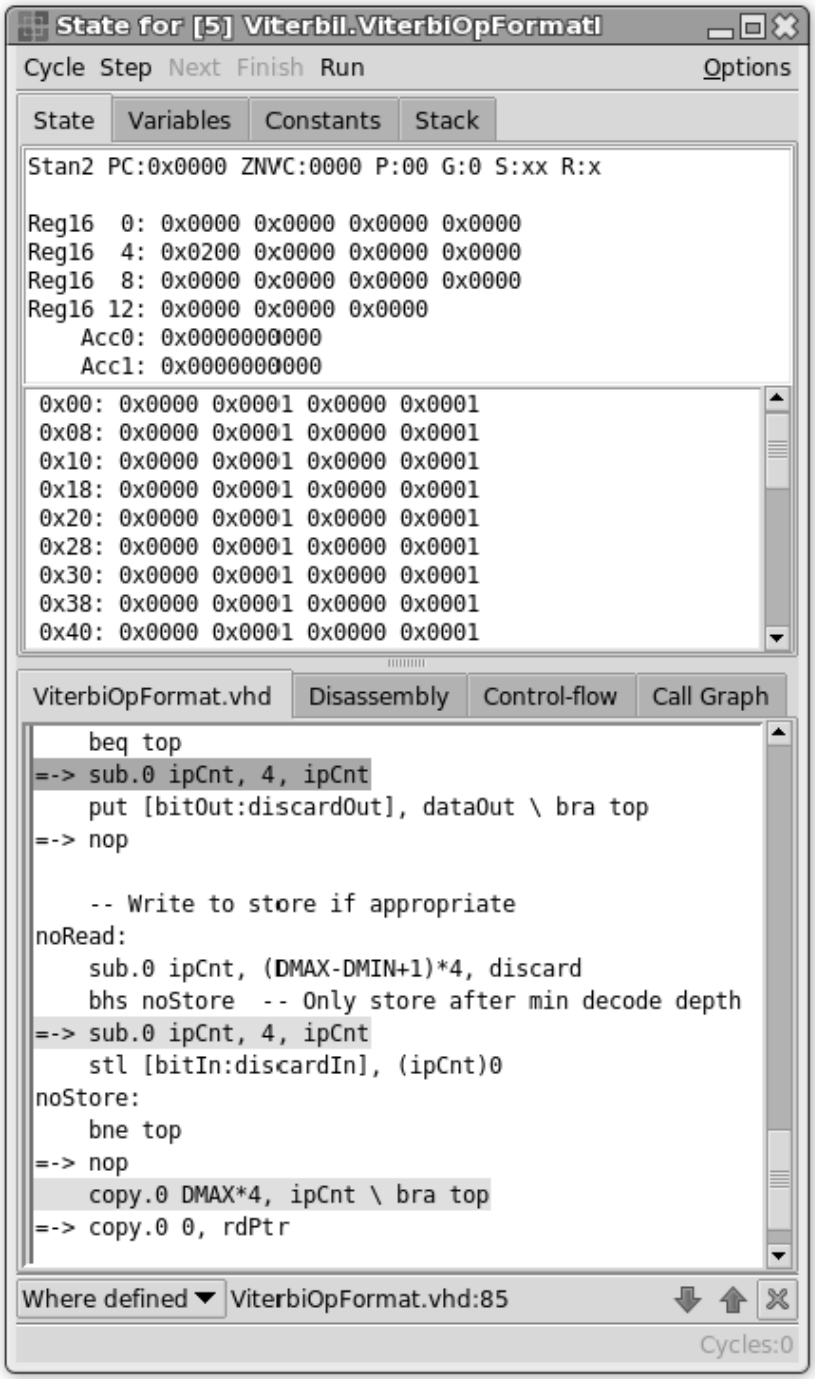


Chapter 5

Debugging Multi-Core Syst

- Debugging tool which allows
  the error





Chapter 6

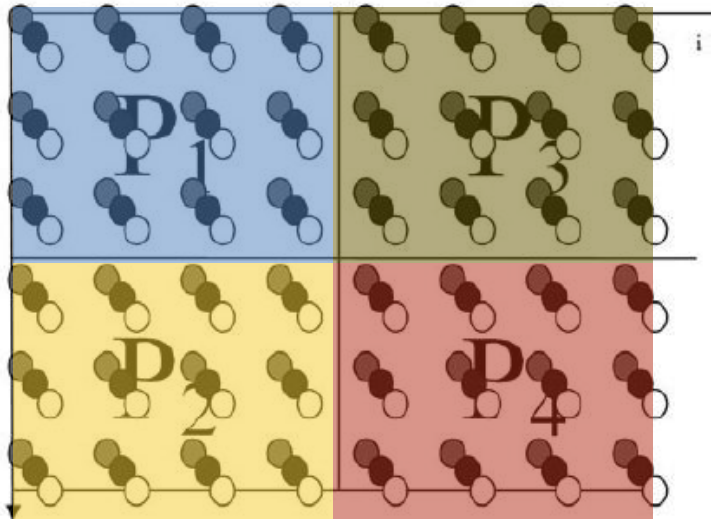
System-Level Tools for NoC-Based Multi-Core Design

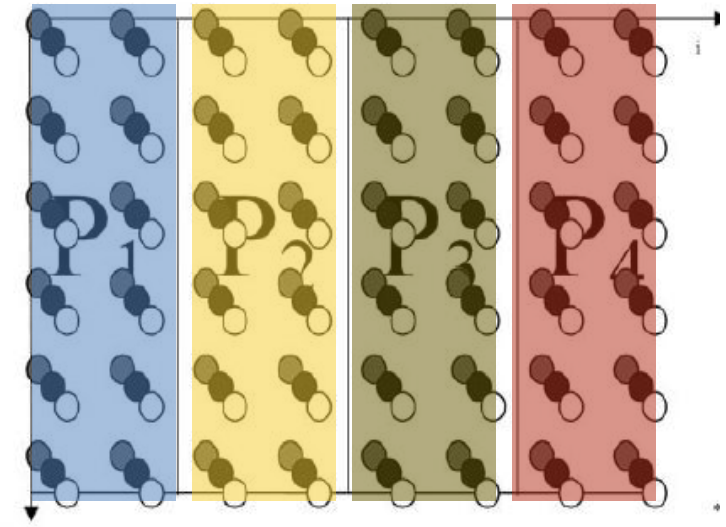
- Theoretical discussion on network topology for NoC
- General graph theory with applications
- Borrowing from other fields: traffic modeling, network simulation, etc.
- SCOTCH tool examples

Chapter 7

Compiler Techniques for Application Level Memory Optimization for MPSoC

- General memory optimization techniques
- Loop transformations
- Partitioning





Chapter 8

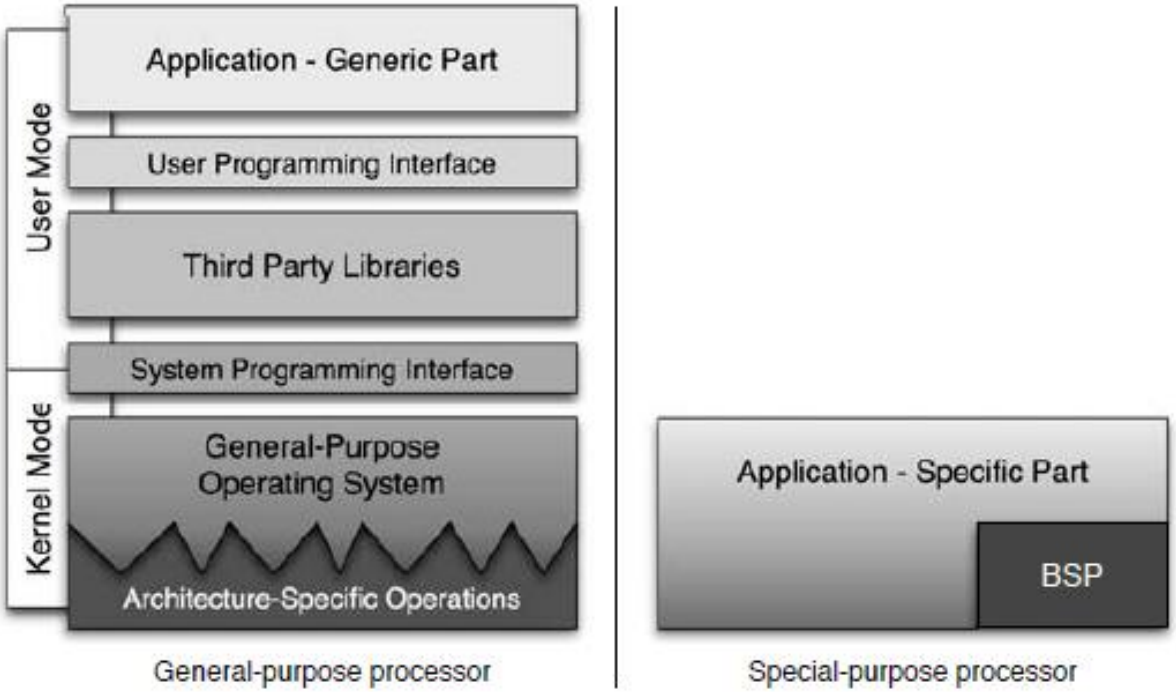
Programming Models for Multi-Core Embedded Software

- Shared memory models: OpenMP
- Distributed memory models: MPI
- Languages designed for parallelism: CUDA, Estral, LUSTRE, SIGNAL (with examples)

Chapter 9

Operating System Support for MCSoC

- Industrial and domain-specific software
- Designing the operating system



Chapter 10

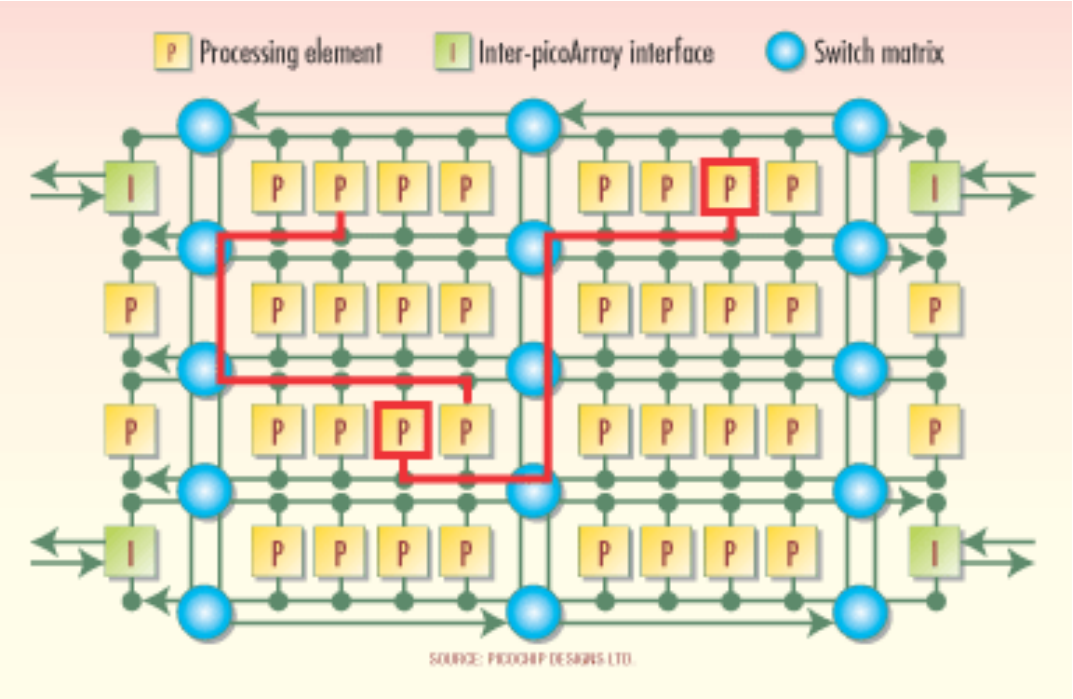
Autonomous Power Management in Embedded Multi-Cores

- More important for embedded multi-cores then the regular CPUs
- CASPER - top-down integrated simulation for MC systems

Chapter 11

MCSoC in Real World Products

- Details about the picoChip and the picoArray
- Tiled architecture (100s processors)



Chapter 12

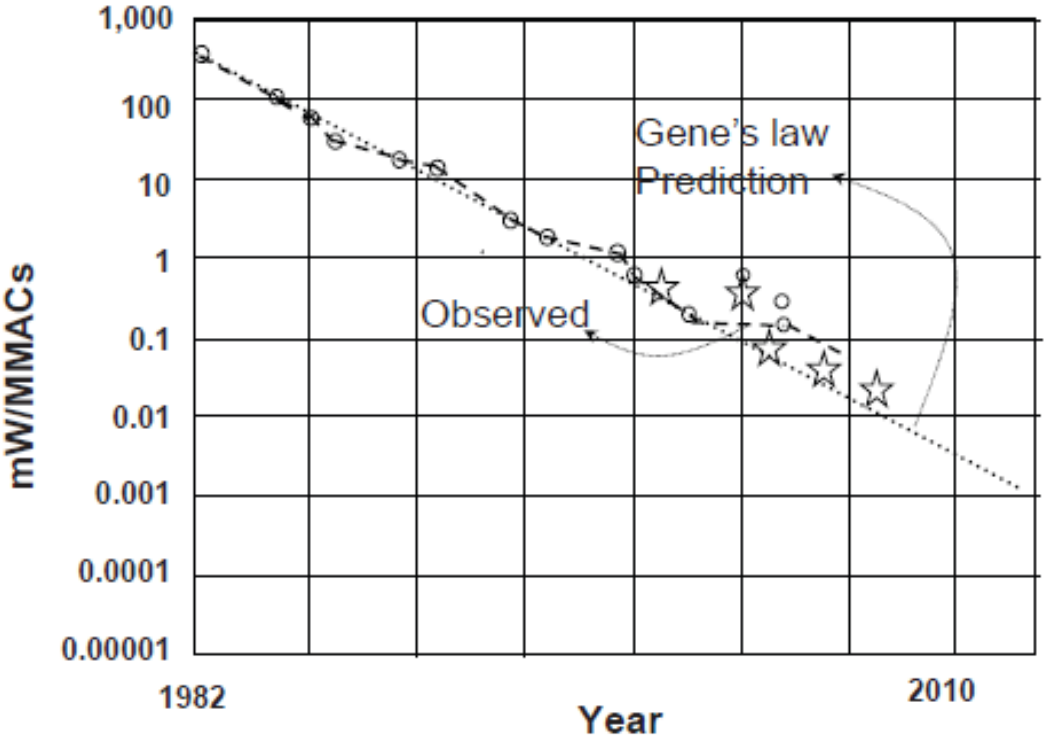
Embedded Multi-Core Processing for Networking

- Network processing units (NPU)
- Fully programmable like DSPs
- Optimized for transmitting packets and cells

CHAPTER 1

What Makes MP Solutions Attractive?

- Power Dissipation



- Hardware Implementation

Power Dissipation in ES Context

- Power dissipation of hand-held devices needs to be controlled. Or else…

- "g ly toda

MP Power Dissipation Advantages

- multiple power domains
  - sub-systems may be turned on/off as dictated by usage
  - I/O interfaces may be turned on/off as needed
- **gated clocking** - clock system for a sub-system can be turned off
- **power gating** - power supply to a sub-system can be turned off

MP Power Dissipation Advantages

- multiple power domains
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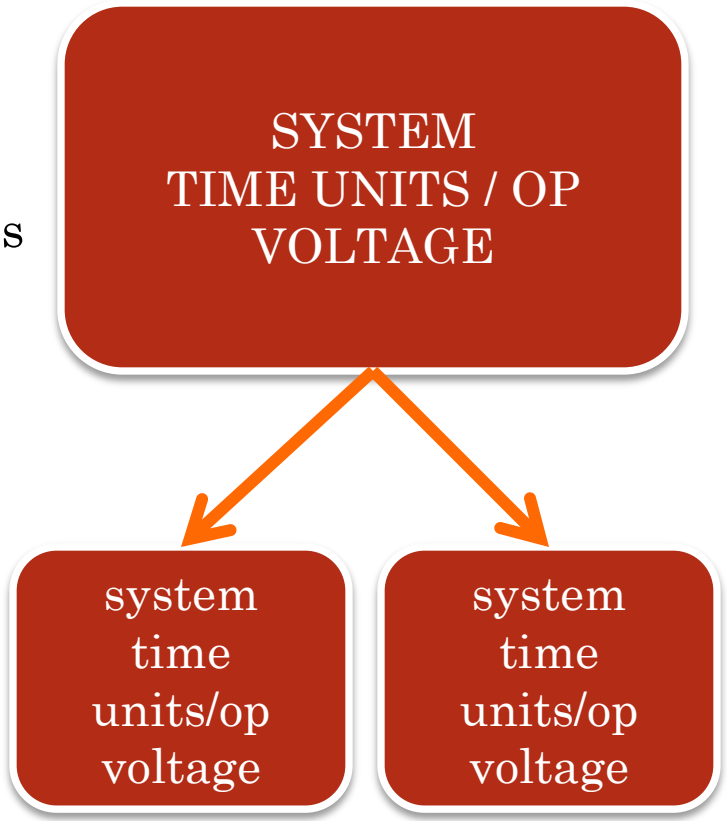
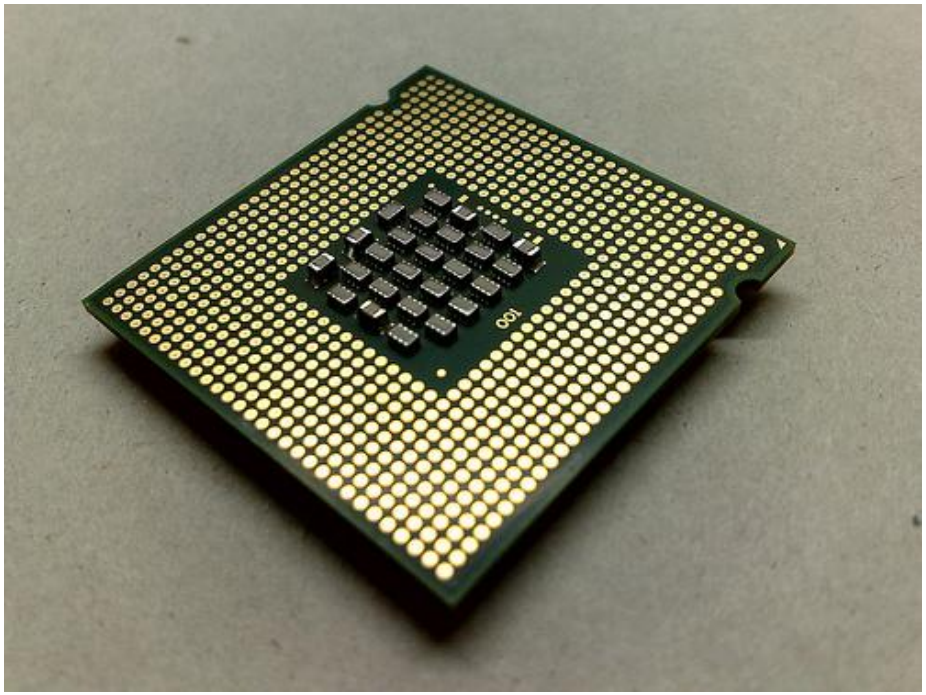
  - I/O interfaces may be turned on/off as needed
- **gated clocking** - clock system for a sub-system can be turned off
- **power gating** - power supply to a sub-system can be turned off
- getting the same number of operations/s with less power



Hardware Implementation

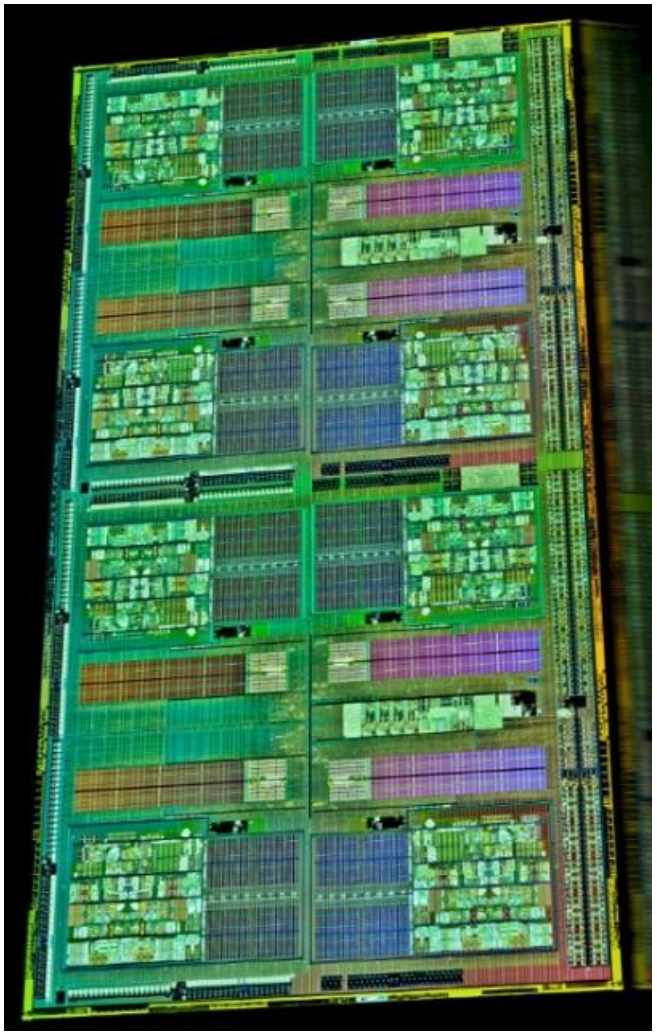
Automated logic design is more efficiently done with small multiple processors rather than single high freq CPUs

- **Timing-closure** problem at high clock speeds
  - Resistance
  - Capacitance
  - Inductance
- Difficult to predict the **critical paths**



Hardware Implementation

- **Divide-and-conquer**
  - design smaller blocks
  - reuse templates
  - control on-chip temperature variability
  - more efficient testing patterns
  - *Replication is your friend*

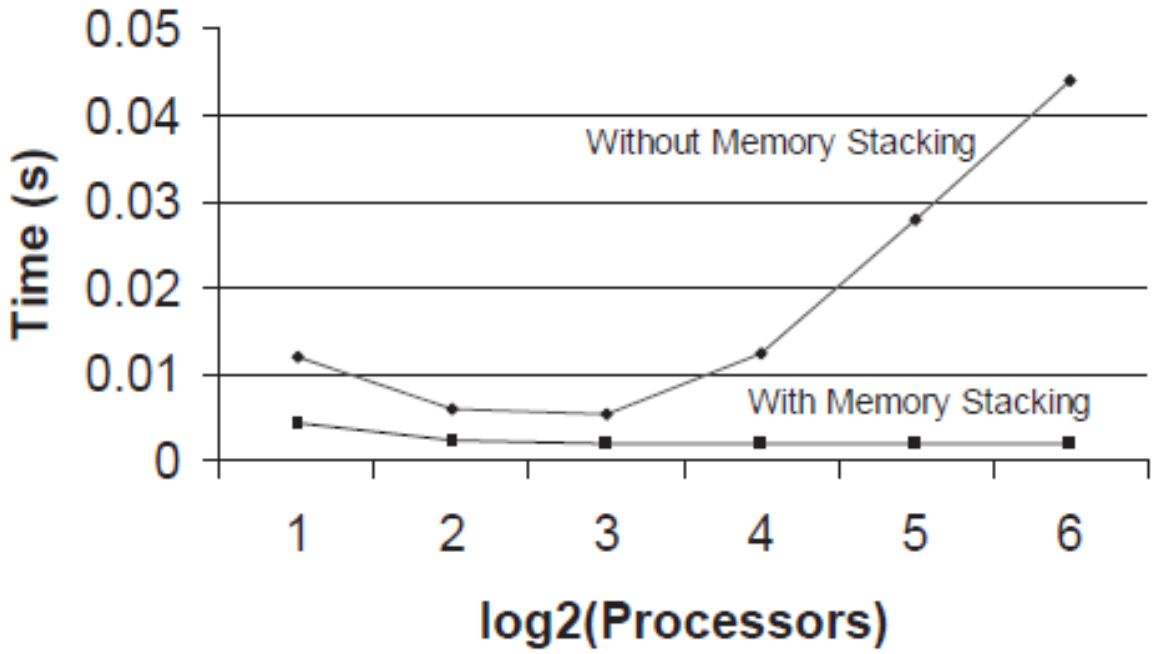


Architectural Design Decisions

Using existing CPU core	Developing a new one
Heterogeneous	Homogeneous
Large number of less powerful CPUs	Small number of powerful CPUs

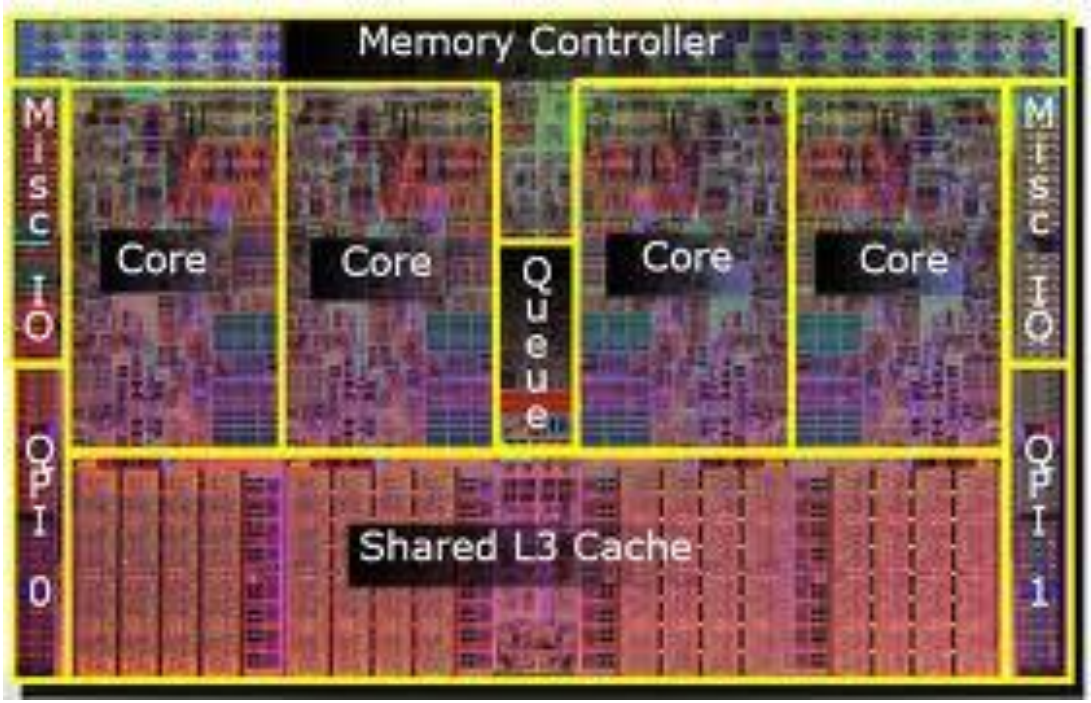
Memory Considerations

- Memory limitations
  - Memory management is the main limiting factor in the performance of parallel machines



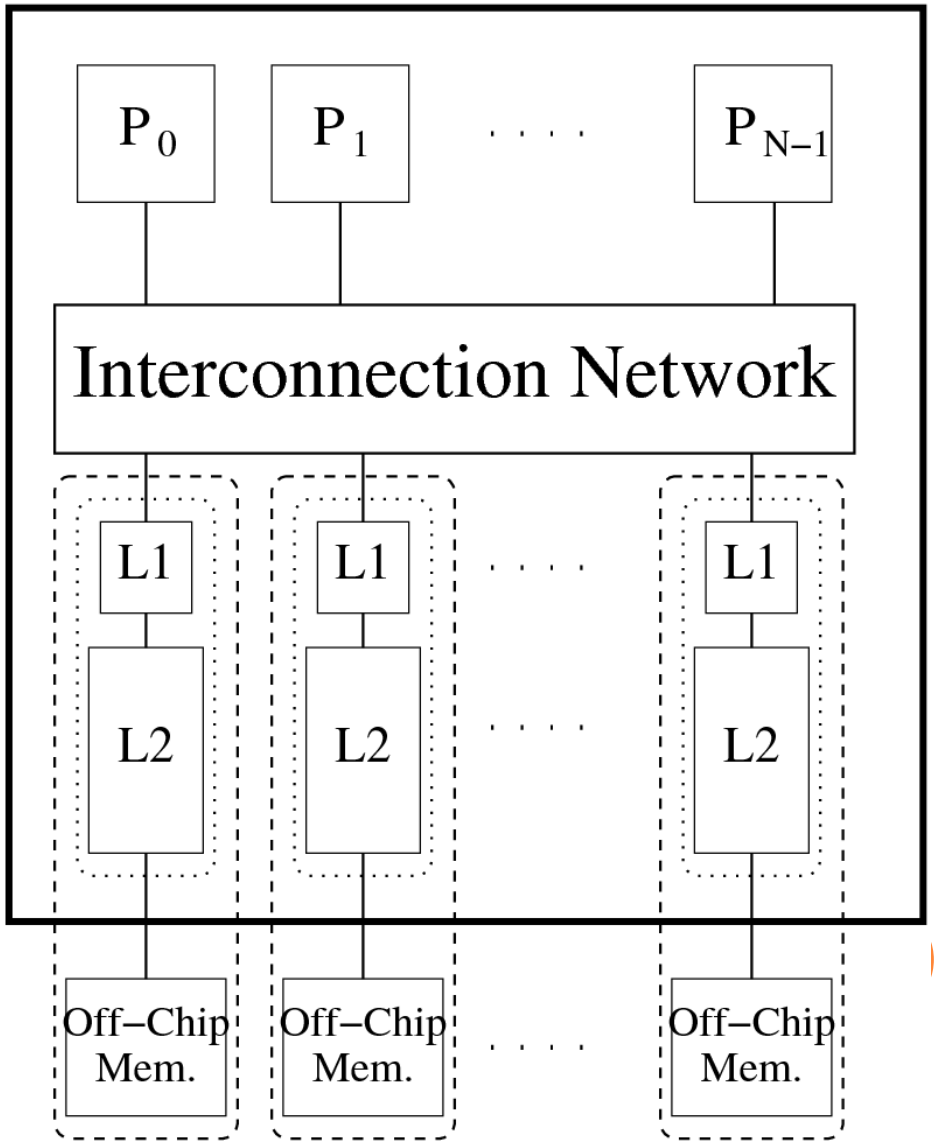
Memory Considerations

- Memory occupies more than 50% of the die area in modern MPSoCs
- Variations:
  - Distributed shared
  - Centrally shared
  - Not shared



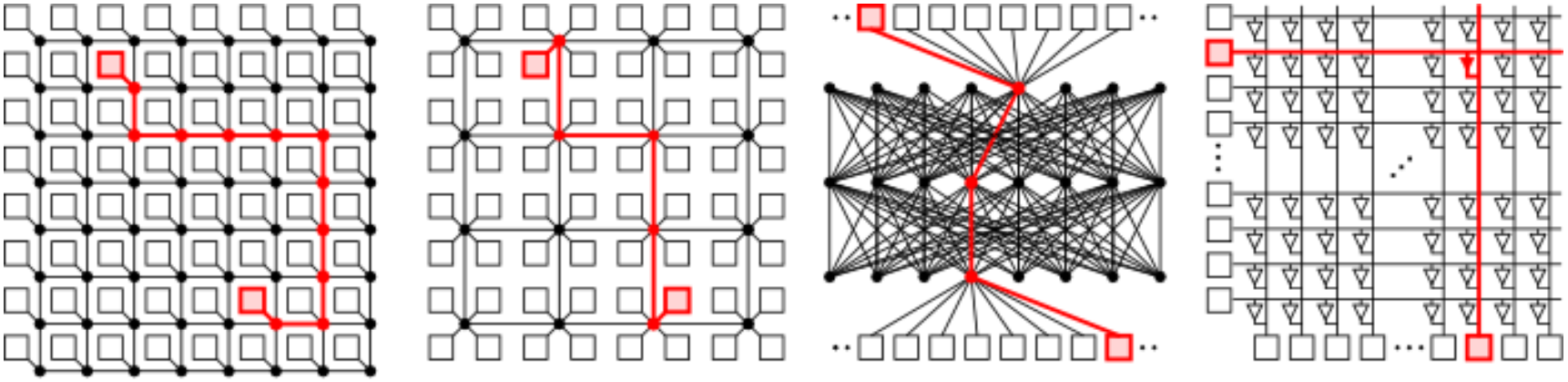
Interconnection Networks

- Major considerations:
  - Propagation delay
  - Testabilty
  - Layout area
  - Expandability



Interconnection Networks

- While the busses are the most popular scheme today, they do no scale well
- A modular approach is needed



http://www.csl.cornell.edu/courses/ece5970/

Network-on-Chip (NoC)

- Globally Asynchronous, Locally Synchronous (GALS)

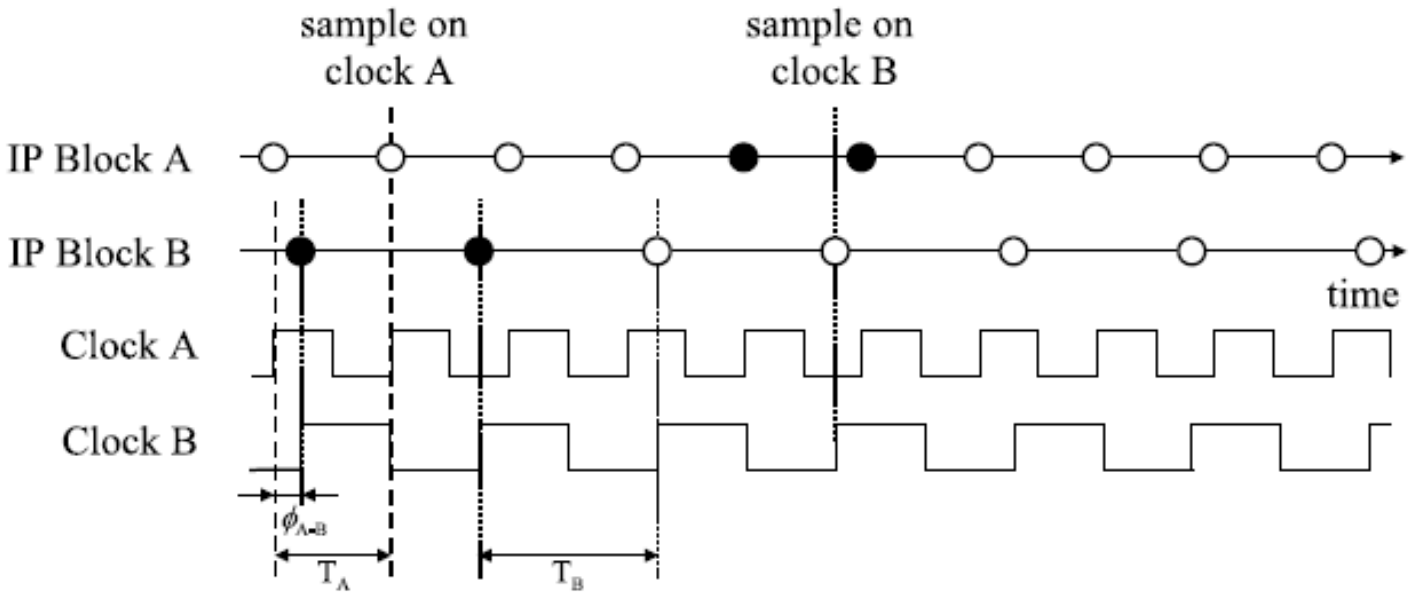


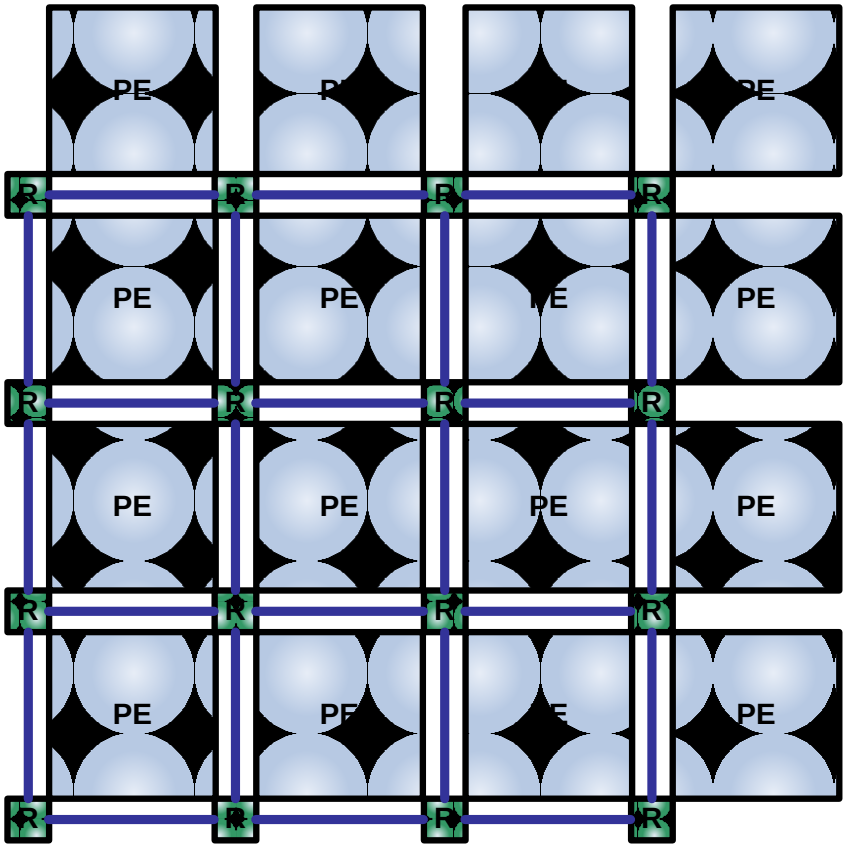
FIGURE 5.3: Lack of consistent global state with multiple, asynchronous clocks.

Network-on-Chip (NoC)

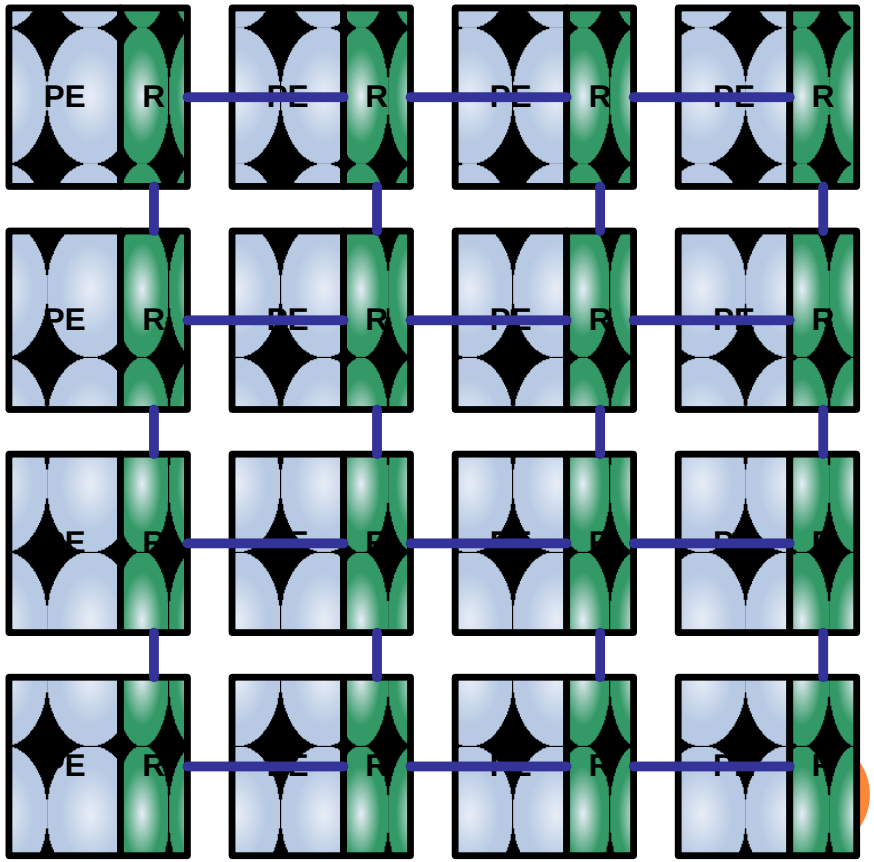
- Globally Asynchronous, Locally Synchronous (GALS)
- Possible Architectures:
  - 2D mesh
  - Tree based architecture
  - Irregular

2D Mesh Topology

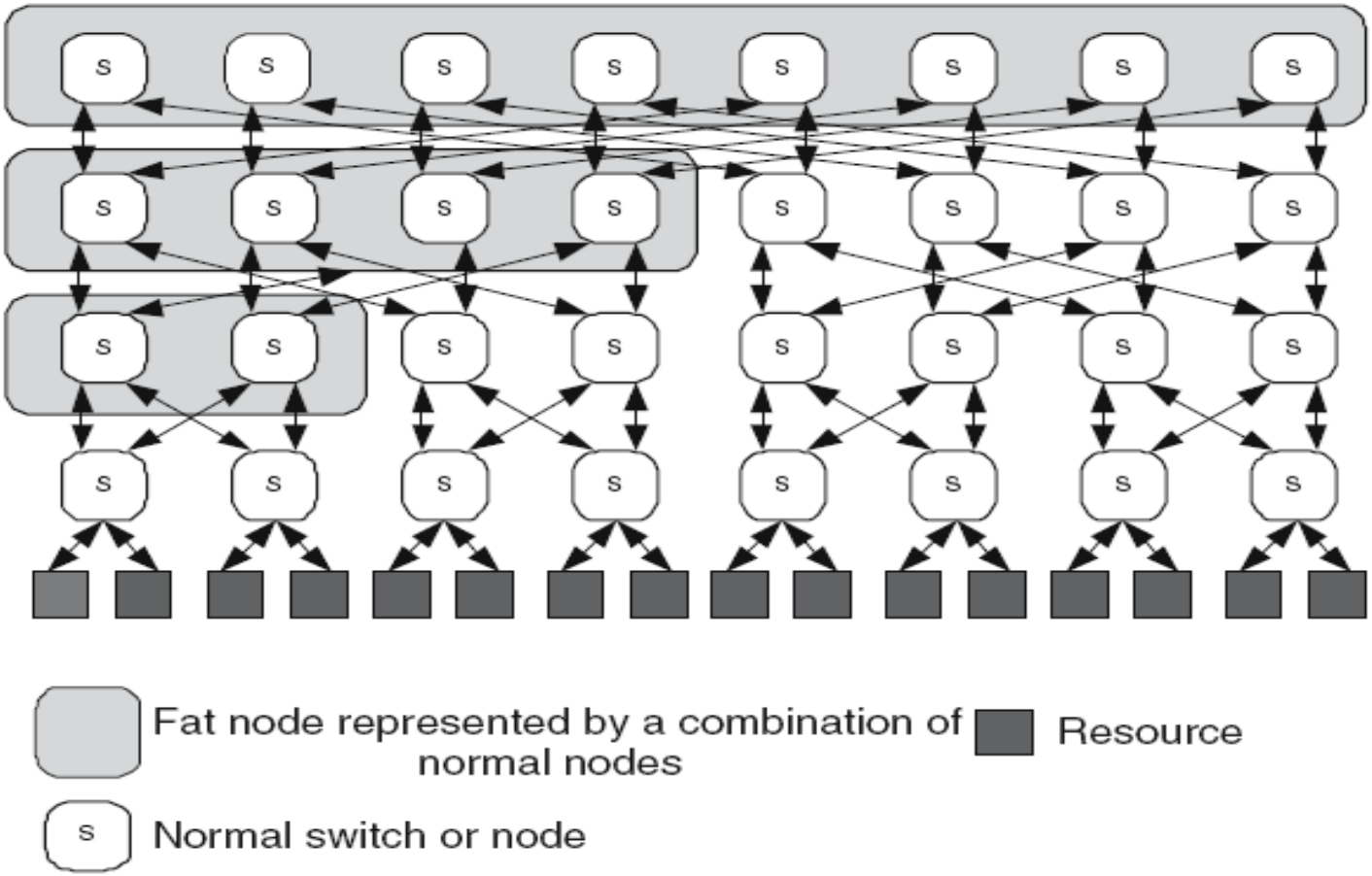
Regular 2D Mesh



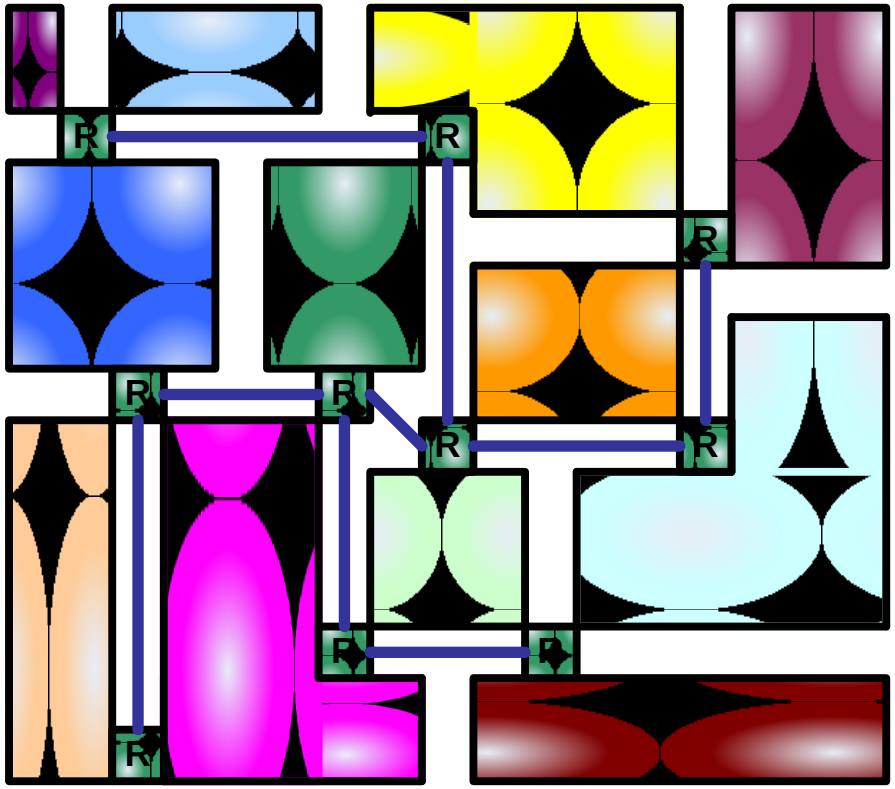
Tiled 2D Mesh



Tree-Based


S
Fat node represented by a combination of normal nodes
Resource
S
Normal switch or node

Irregular Topology



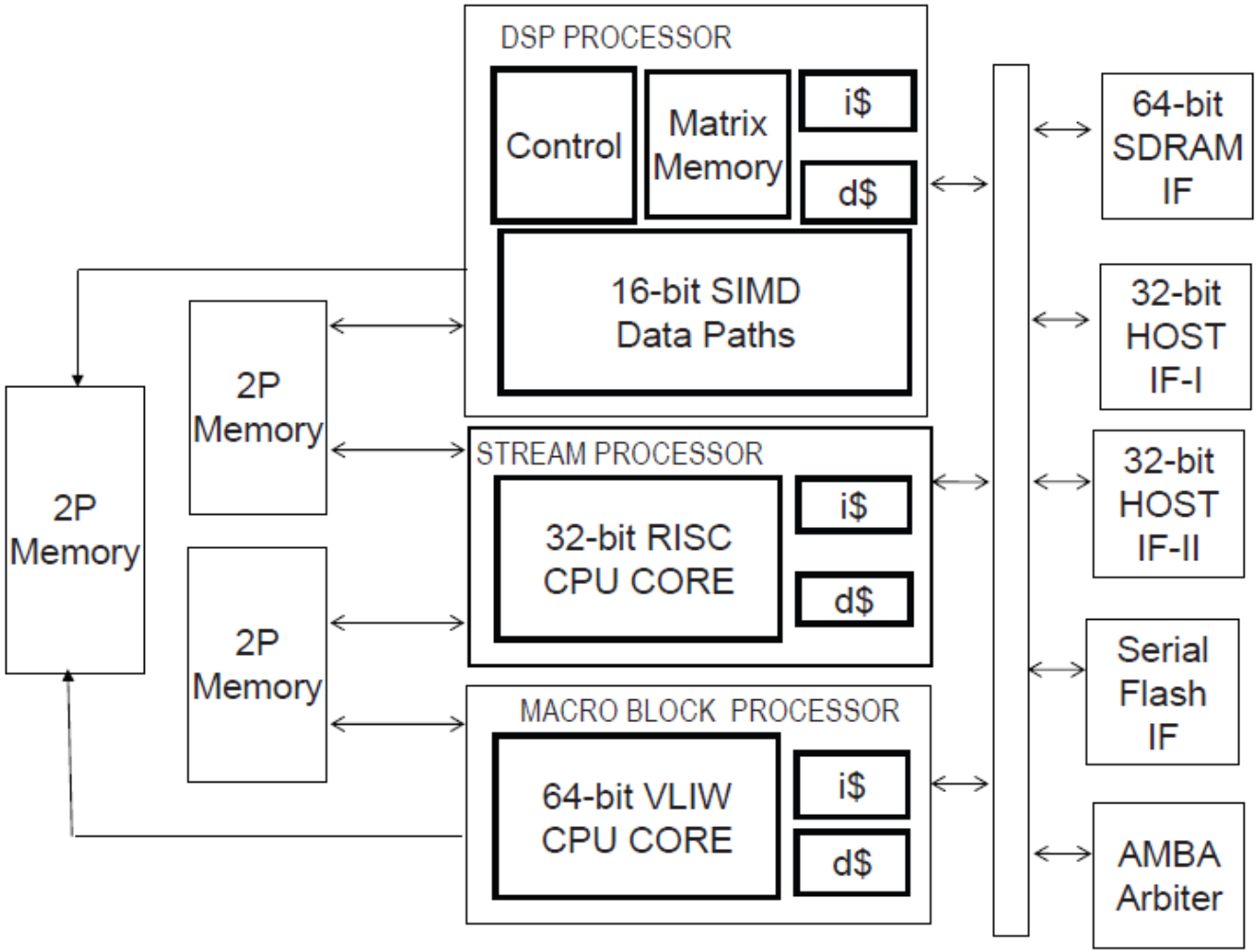
Software Optimizations

- extracting parallelism
  - coarse grain - person
  - fine grain – compiler
  - vendors usually provide models and simulation tools
- task allocation and scheduling
  - genetic algorithm is popular for this
- management of inter-processor communication (including memory and i/o management)
  - challenging problem - no easy solution yet

EXAMPLES OF MP EMBEDDED ARCHITECTURES

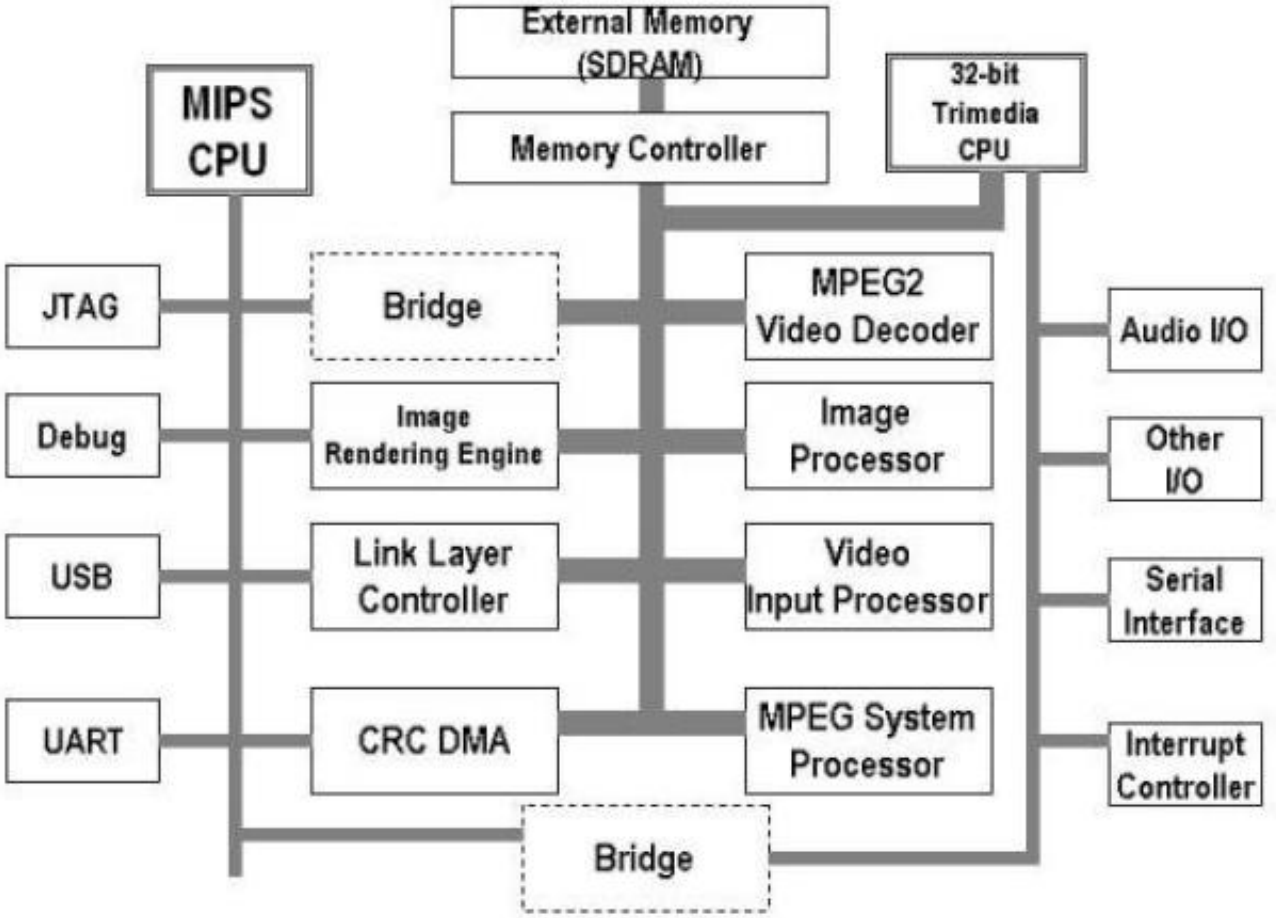
HiBRID-SoC for Multimedia Signal Processing

- Processors
  - HiPAR-DSP
  - RISC stream processor
  - Special processor for video



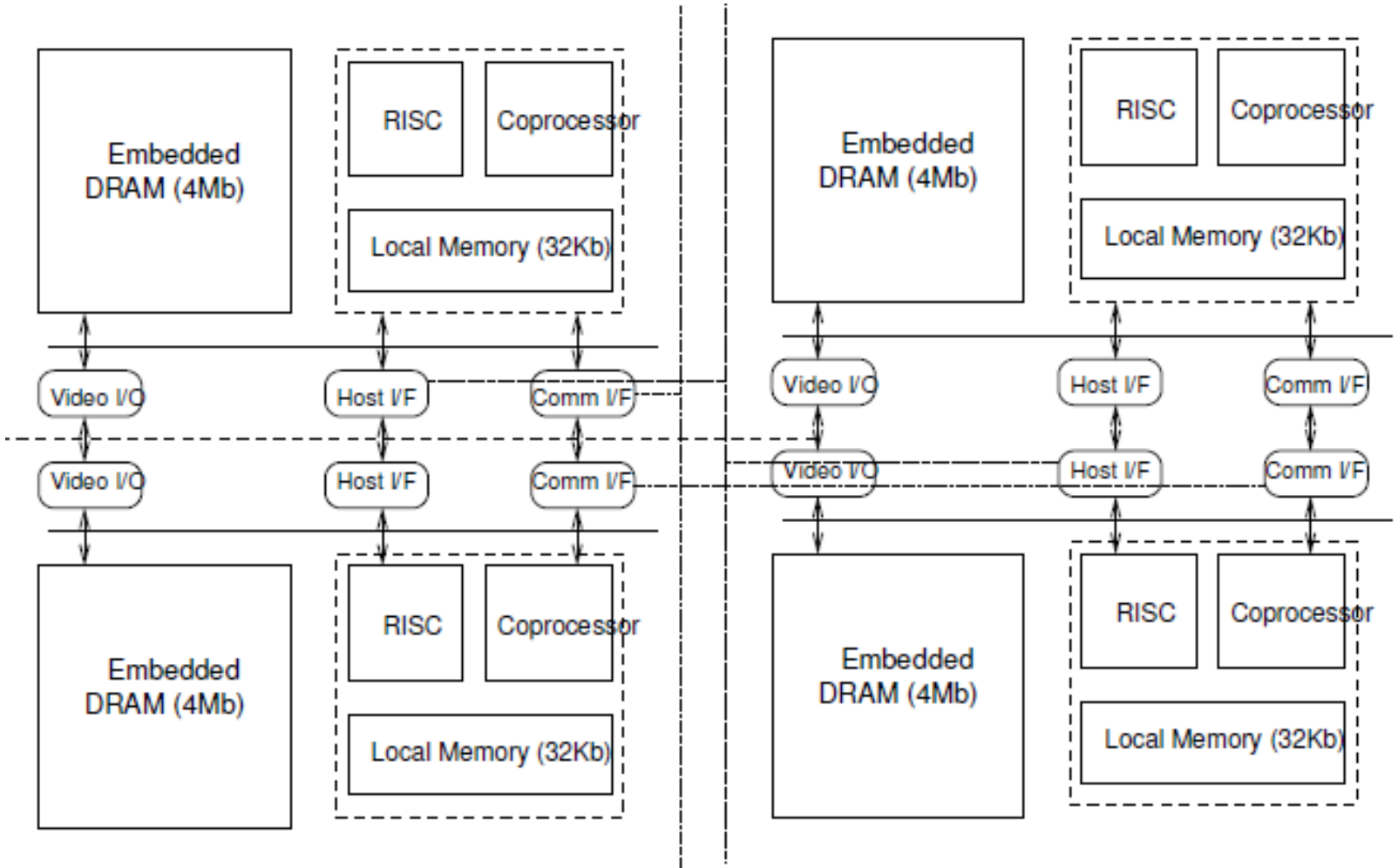
VIPER MULTIPROCESSOR SOC

- Heterogeneous (For set-top boxes)



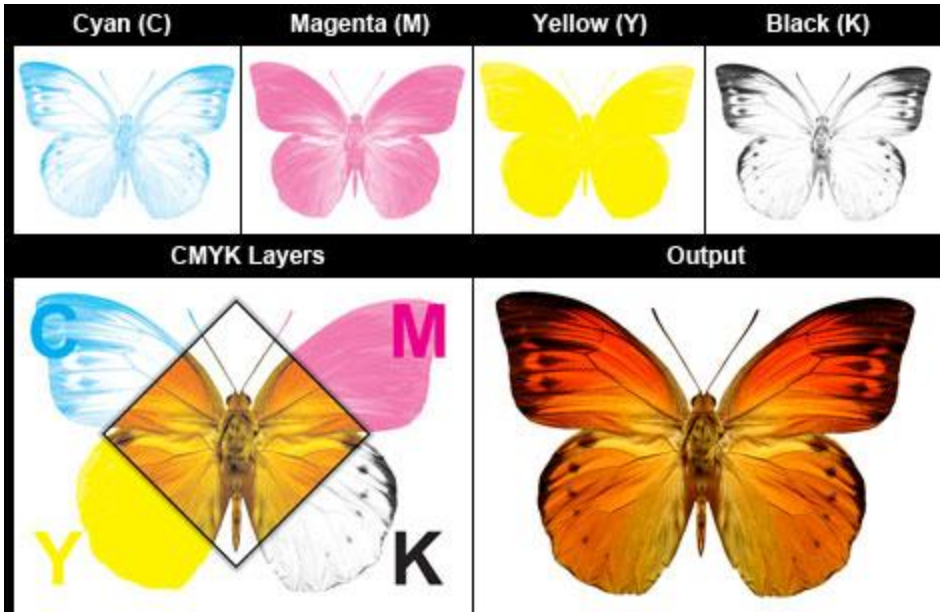
Defect-Tolerant and Reconfigurable MPSoC

- Digital video and satellite communication



Homogeneous Multiprocessor for Embedded Printer Application

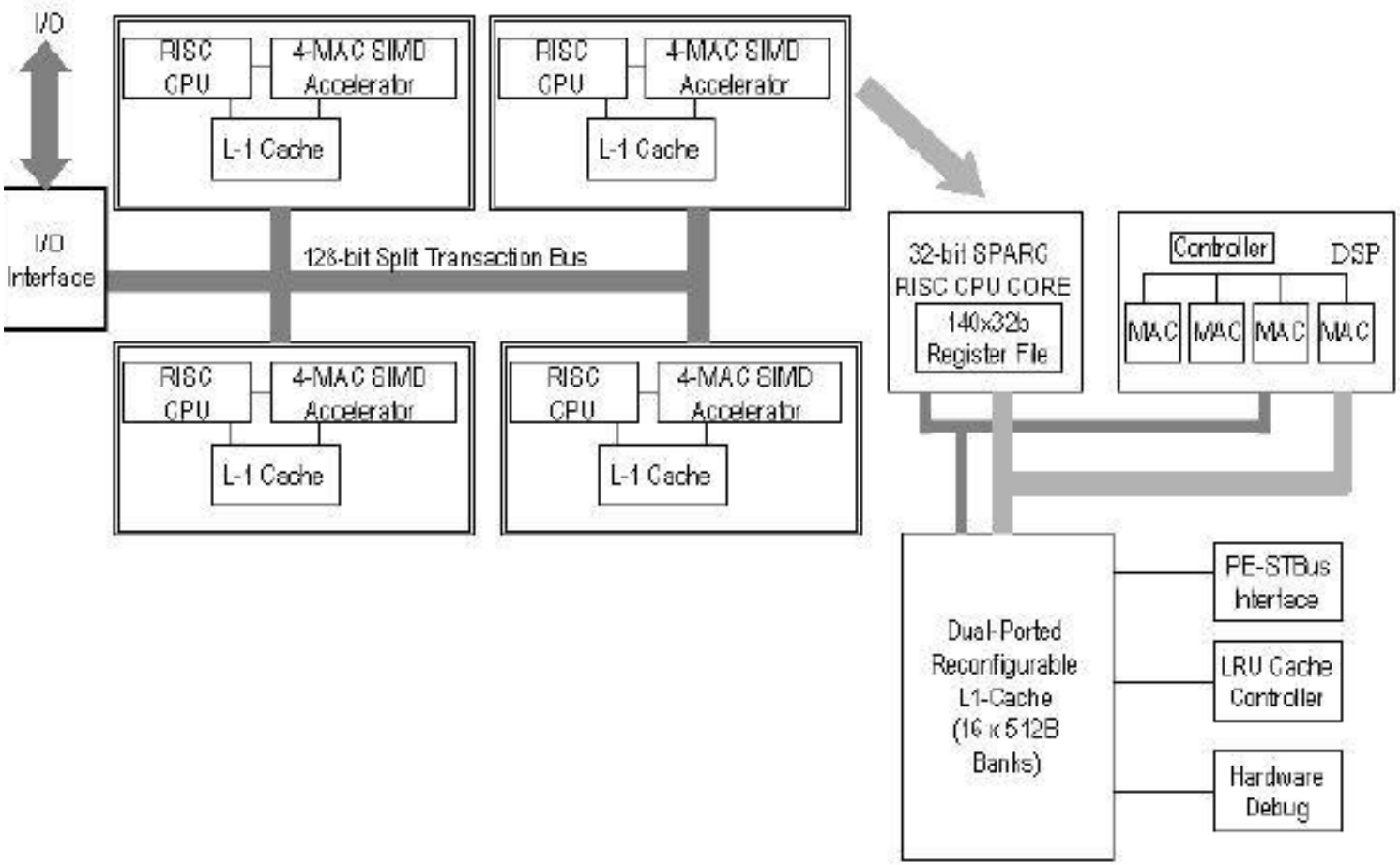
- Printers process in chunks called “strips”
- Lends itself to coarse-grained parallelization



<table>
<tr><td colspan="8">Four Banks of Embedded DRAM
(Size = 1MB per bank)</td></tr>
<tr><td colspan="8">256–bit BUS at 256 MHz</td></tr>
<tr><td>i$</td><td>d$</td><td>i$</td><td>d$</td><td>i$</td><td>d$</td><td>i$</td><td>d$</td></tr>
<tr><td colspan="2">CPU1</td><td colspan="2">CPU2</td><td colspan="2">CPU3</td><td colspan="2">CPU4</td></tr>
</table>

General Purpose Multiprocessor DSP

- Daytona design built for scalability
  - Split transaction bus



Final Thoughts

- This book is freely available online (yes, legally)
- Most of the material looks to be applicable to general multi-core architectures
  - Good parallel coding practices
  - Memory issues
  - Design considerations
- Embedded System Examples
  - Seem a bit “extra”

Questions

Thank You